AMENDMENTS TO THE SPECIFICATION:

Please amend the title as follows:

--SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH BOUNDARY SCAN TEST AND DESIGN AUTOMATION APPARATUS, BOUNDARY SCAN TEST METHOD AND PROGRAM--

Please replace the Abstract of the Disclosure with the following rewritten Abstract which appears on a separate sheet in the Appendix.

Page 1, replace the paragraph beginning on line 18 and bridging pages 1 and 2 with the following amended paragraph:

--Fig. 1 is a diagram illustrating the schematic structure of a typical boundary-scan circuit (see, for example, "Fundamentals and Application of JTAG Test" by Kazumi Sakamaki, p 24, Fig. 2-2, CQ Publication Co., Ltd., December 1, 1998). A boundary-scan register has a multiplexer M1, a flip-flop F1, a flip-flop F2, and a multiplexer M2. The multiplexer M1 receives a serial signal input SI and a signal input PI and selects the input SI in response to a Shift_DR command (signal S). The flip-flop F1 samples the output of the multiplexer M1 according to a shift clock and outputs a sampled signal as SO. The flip-flop F2 samples the output of the flip-flop F1 according to an update clock (Update_DR) and outputs a sampled signal. The multiplexer M2 receives the output of the flip-flop F2 and the signal PI and outputs one of the inputs to a terminal PO based on a mode signal MODE. In case of an input cell, the terminal PI is connected to

the input pin and the terminal PO to an internal circuit. In case of an output cell, the terminal PI is connected to the internal circuit and the terminal PO to the output pin. An input/output cell takes such a structure as to have two circuits each as shown in Fig. 2 which are switched from one to the other in accordance with the input and the output. The serial input terminal SI receives TDI (Test Data Input) or an output TDO (Test Data ~~Input~~ Output) of the boundary-scan circuit at the previous stage.--

Page 4, replace the paragraph beginning on line 20 with the following amended paragraph:

--In test mode, the pins of the device are isolated from the internal circuit and test signals are supplied to the boundary-scan registers. Each boundary-scan register serves a shift register and outputs a signal input from the unillustrated TDI terminal to the unillustrated TDO terminal. In the example shown in Fig. 2, each I/O cell has such a structure as to include the control circuit 21, 22 or ~~so~~ the like for the boundary-scan test and some I/O cells have buffers 23 for enabling the global wirings.--

Page 5, replace the paragraph beginning on line 1 with the following amended paragraph:

--As fan-out adjustment of a test net which passes through the boundary-scan register, the following method (Japanese Patent Laid-Open No. 2002-26129) is known. According

to the method, after the layout of I/O cells, I/O connection boundary-scan registers are laid out in empty areas near the I/O cells by priority before laying out an internal logic circuit or ~~so~~ the like, an I/O control boundary-scan register is laid out at the midway point between the I/O connection boundary-scan registers or the side of the chip closer to the midway point, then buffer cells are laid out in test nets corresponding to the boundary-scan registers connected to the test control circuits before creating the layout and wiring patterns of cells which constitute other circuits, whereby fan-out adjustment between the test control circuits and the boundary-scan registers is executed with the minimum number of buffers inserted. Unlike the conventional method, the present invention inserts a buffer in an empty cell in the I/O area as will be apparent from the description of the present invention given later.--

Page 6, replace the paragraph beginning on line 13 with the following amended paragraph:

--Accordingly, it is an object of the present invention to provide a suitable semiconductor integrated circuit device adaptable for an ASIC or ~~so~~ the like, which can suppress an increase in the delay of a test signal to be transferred along the chip's peripheral portion and degradation in waveform depression and can ensure delay adjustment, and a method, apparatus and program for design automation of the semiconductor integrated circuit device.--

Page 6, replace the paragraph beginning on line 21 and bridging pages 6 and 7 with the following amended paragraph:

--A semiconductor integrated circuit device according to the first aspect of the present invention comprises ~~a predetermined~~ plural I/O cells provided in an I/O area in a peripheral portion of a chip ~~and~~ that are to be connected to external pins; signal wirings which transfer a test signal to the I/O cells and are provided in the I/O area in a layout direction of the plurality of I/O cells; and at least one ~~empty cell~~ part of the I/O area where the signal wirings run and ~~which is to be a transfer path for the test signal, is provided in the I/O area and~~ that does not include I/O cells has a repeater circuit therein that receives the test signal and outputs the test signal.--

Page 7, replace the paragraph beginning on line 4 with the following amended paragraph:

--According to the present invention, ~~when there is empty space in the I/O area for a single empty cell or plural cells,~~ the ~~optimal~~ repeater circuit ~~that has the characteristic satisfying at least a predetermined signal~~ satisfies a delay condition ~~is selected from plural types of repeater circuits, provided beforehand, different from one another in electrical characteristics and is laid out as a repeater circuit for the empty cell either in the empty space for a single cell or the empty space for plural cells~~ of the test signal.--

Page 7, replace the paragraph beginning on line 13 and bridging pages 7 and 8 with the following amended paragraph:

--A design automation apparatus for a semiconductor integrated circuit according to the second aspect of the present invention comprises: a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O ~~cells~~ cell on a chip which are to be connected to external pins; a computing section which computes a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be connected to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to said I/O cell layout position information, I/O cell size information and I/O cell test terminal information in said memory unit and outputs said wiring length; a circuit simulator; a determining section which computes information at least on a wiring resistance and a capacitance for said sub net, causes said circuit simulator to execute circuit simulation to acquire a wiring delay of said sub net and waveform depression at an end of said sub net, and determines an optimal repeater circuit to be inserted in an empty cell where said sub net passes, based on said information on said repeater circuit stored in said memory unit in case where said wiring delay and waveform depression concerning said sub net are out of a

predetermined range of allowance defined in said technology information; and a layout section which lays out an empty cell including said determined repeater circuit in said I/O area.--

Page 8, replace the paragraph beginning on line 14 with the following amended paragraph:

--According to the design automation apparatus of the present invention, the determining section determines a repeater circuit may include means which performs control in such a way as to execute circuit simulation for a sub net divided by insertion of a selected repeater circuit to acquire a wiring delay and waveform depression concerning the divided sub net, determine whether the wiring delay and waveform depression concerning the divided sub net fall within the range of allowance defined in the technology information or not, and search for an ~~optical~~ optimal repeater circuit by selecting another repeater circuit or further dividing the sub net in case where the wiring delay and waveform depression do not fall within the range of allowance.--

Page 8, replace the paragraph beginning on line 28 and bridging pages 8 and 9 with the following amended paragraph:

--According to the third aspect of the present invention, there is provided a design automation method for a semiconductor integrated circuit using a computer having a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a

repeater circuit to be laid out in an empty cell for each type of I/O ~~cells~~ cell on a chip which are to be connected to external pins. The method comprises the steps of computing a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be connected to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to the I/O cell layout position information, I/O cell size information and I/O cell test terminal information in the memory unit and outputting the wiring length; computing information at least on a wiring resistance and a capacitance for the sub net, causing ~~the~~ a circuit simulator to execute circuit simulation to acquire a wiring delay of the sub net and waveform depression at an end of the sub net; a step of determining an optimal repeater circuit to be inserted in an empty cell where the sub net passes, based on the information on the repeater circuit stored in the memory unit in case where the wiring delay and waveform depression concerning the sub net are out of a predetermined range of allowance defined in the technology information; and laying out an empty cell including the determined repeater circuit in the I/O area.--

Page 9, replace the paragraph beginning on line 28 and bridging pages 9 and 10 with the following amended paragraph:

--According to the design automation method of the present invention, the step of determining a repeater circuit may include the steps of performing control in such a way as to

execute circuit simulation for a sub net divided by insertion of a selected repeater circuit to acquire a wiring delay and waveform depression concerning the divided sub net; and determining whether the wiring delay and waveform depression concerning the divided sub net fall within the range of allowance defined in the technology information or not, and searching for an ~~optical~~ optimal repeater circuit by selecting another repeater circuit or further dividing the sub net in case where the wiring delay and waveform depression do not fall within the range of allowance.--

Page 10, replace the paragraph beginning on line 14 and bridging pages 10 and 11 with the following amended paragraph:

--According to the fourth aspect of the present invention, there is provided a program embodied in a computer-readable medium for allowing a computer having a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O ~~cells~~ cell on a chip, which are to be connected to external pins, to execute a first process of computing a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be wired to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to the I/O cell layout position information, I/O cell

size information and I/O cell test terminal information in the memory unit and outputting the wiring length; a second process of computing information at least on a wiring resistance and a capacitance for the sub net, causing ~~the~~ a circuit simulator to execute circuit simulation to acquire a wiring delay of the sub net and waveform depression at an end of the sub net; a third process of determining an optimal repeater circuit to be inserted in an empty cell where the sub net passes, based on the information on the repeater circuit stored in the memory unit in case where the wiring delay and waveform depression concerning the sub net are out of a predetermined range of allowance defined in the technology information; and a fourth process of laying out an empty cell including the determined repeater circuit in the I/O area.--

Page 12, between lines 20 and 22, insert the following paragraph:

--Fig. 10 is a diagram showing an embodiment of the design automation apparatus of the present invention.--

Page 14, replace the paragraph beginning on line 17 and bridging pages 14 and 15 with the following amended paragraph:

--Referring to Fig. 4, an I/O area 40 in the peripheral portion of a chip 1 is provided with, as I/O cells, an input buffer 11 which connects to an input pin 51 and an output buffer 12 which connects to an output pin 52, and is further provided with a power supply block (cell) 18 which connects to a power

supply terminal ~~(VDDy)~~ (VDD) 53 and ground (GND) block 19 which connects to a GND terminal 54. Corner cells 14 which constitute test control circuits are provided at the corners of the chip. The chip 1 is further provided with boundary-scan terminals (TDI, TMS, TCK, TDO, TRST) and scan path test terminals (SIN, SCK, SOT) none of which are shown. Empty cells 15 each having a repeater circuit to compensate for signal delay of a test net are provided in an empty area in the I/O area 40 where the I/O cells and cells, such as power supply block and GND block, are not provided.--

Page 18, replace the paragraph beginning on line 15 and bridging pages 18 and 19 with the following amended paragraph:

--Fig. 7 is a diagram illustrating one example of the structure of the output buffer 12. A boundary-scan register 121 receives the parallel input signal PIN (data input DIN from the internal circuit), serial input signal BSIN, shift data register (Shift_DR) signal SFDR and shift clock signal CLKDR, outputs the serial output BSOUT and outputs data, selected by a multiplexer (M2 in Fig. 1) from a parallel output terminal PO. The output BSOUT is either supplied to the serial input BSIN of the next cell or output from the TDO pin of the device in case of the last-stage cell in the scan chain in the device. A scan flip-flop circuit 122 is a known scan flip-flop circuit which has a data terminal D to receive data DIN from an internal circuit, a clock terminal C to receive a sampling clock for sampling a

signal from the data terminal D at the rising edge, a normal output terminal Q, 2-phase scan clock terminals SC1 and SC2, a serial input terminal SIN, a serial output terminal SOUT, a reset terminal RB and a set terminal SB. A logic circuit 124 receives SB and SMC2 which are test control signals and performs such control as to enable the set terminal SB of the scan flip-flop circuit 112 to set the output of the set terminal SB to logic 1, for example, when the signal SB is at a low level and the signal SMC2 is at a high level. A logic circuit 126 receives RB and SMC2 which are test control signals and performs such control as to enable the reset terminal RB of the scan flip-flop circuit 122 to reset the output of the reset terminal RB to logic 0 when the signal RB is at a low level and the signal SMC2 is at a high level. The logic circuits 124 and 126 may each be constituted by an SR flip-flop which sets its output terminal S to a low level when its terminal SETB is at a low level and sets the output terminal S to a high level when its terminal SMC2 is at a low level. A circuit 125 is designed in such a way as to supply a normal clock signal CLK to the clock terminal C of the scan flip-flop circuit 112 when its terminal SCN is active. A multiplexer 123 receives a data output Q (parallel output) of the scan flip-flop circuit 122 and a parallel output PO of the boundary-scan register 121, and outputs the data output Q of the scan flip-flop circuit 122 as DOUT when the mode signal MODE has a logic ~~0and~~ Ø and outputs the parallel output PQ of the scan boundary-scan

register 121 as DOUT when the mode signal MODE has a logic 1.--

Page 20, replace the paragraph beginning on line 2 with the following amended paragraph:

--The operation of the ~~input~~ output buffer illustrated in Fig. 7 is briefly described. In normal operation mode, the data DIN is latched by the scan flip-flop circuit 122 and output as DOUT. In scan path test mode, the scan flip-flop circuit 122 samples the serial input SIN by means of a master-slave latch circuit which is controlled according to scan clocks SC1 and SC2, and outputs the serial output SOUT. In boundary-scan test mode, the signal BSIN is output as BSOUT under the control of the unillustrated TAP controller. When the mode signal MODE has logic 1, a flip-flop F2 (see Fig. 1) of the boundary-scan register 121 is output as DOUT.--

Page 23, insert the following between lines 3 and 4 as follows:

--As shown in Figure 10, the design automation apparatus may include a memory unit 150 which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O cell on a chip which are to be connected to external pins; a computing section 152 which computes a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be connected to

an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to the I/O cell layout position information, I/O cell size information and I/O cell test terminal information in the memory unit and outputs the wiring length; a circuit simulator 154; a determining section 156 which computes information at least on a wiring resistance and a capacitance for the sub net, causes the circuit simulator to execute circuit simulation to acquire a wiring delay of the sub net and waveform depression at an end of the sub net, and determines an optimal repeater circuit to be inserted in an empty cell where the sub net passes, based on the information on the repeater circuit stored in the memory unit in case where the wiring delay and waveform depression concerning the sub net are out of a predetermined range of allowance defined in the technology information; and a layout section 158 which lays out an empty cell including the determined repeater circuit in the I/O area.--

Page 25, replace the paragraph beginning on line 27 and bridging pages 25 and 26 with the following amended paragraph:

--In case where the delay and waveform depression are off the range of the predetermined design condition, on the other hand, division of the sub net 73 is executed and a repeater circuit <u>80</u> comprised of two inverters is inserted in the wiring 73. That is, in case where an empty cell is located between adjoining I/O cells, a single repeater circuit is selected from

the empty cell repeater information 207 and inserted in the empty cell. Then, circuit simulation is performed again on a divided sub net generated through division by the inserted repeater circuit to thereby acquire the wiring delay of the divided sub net and waveform depression at the end. In case where the original sub net is divided into two sub nets, for example, the inverter 72 in Fig. 9 corresponds to an input-stage inverter INV1 of the repeater circuit in the first divided sub net, and the inverter 71 in Fig. 9 corresponds to an output-stage inverter INV2 of the repeater circuit in the second divided sub net. The sub net wiring 73 corresponds to a divided sub net.--